

Application Note 2155 DS80C400 PHY Reset

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INTRODUCTION

The DS80C400 high-speed microcontroller has a built-in Ethernet media-access controller (MAC) with an industrystandard media-independent interface (MII). Please refer to the DS80C400 data sheet and the *High-Speed Microcontroller User's Guide: DS80C400 Supplement* at <u>www.maxim-ic.com/microcontrollers</u> for complete details.

There is a potential timing issue causing problems with the Ethernet receiver when a physical interface (PHY) such as the Intel LXT972ALC is connected to the reset output (RSTOL) of the DS80C400. The solution is to not connect the reset line but instead perform a software reset of the PHY. This application note describes the code necessary to perform a software reset of the PHY.

DS80C400 MAC SOFTWARE LIBRARY

Code to access the DS80C400 MAC and external PHYs is available on our ftp site at <u>ftp://ftp.dalsemi.com/pub/tini/ds80c400/ethdriver/</u> and documented in *Application Note* 712: DS80C400 Ethernet Drivers, available at <u>www.maxim-ic.com/appnoteindex</u>.

PHY SOFTWARE RESET PROCEDURE

The IEEE Standard 802.3 defines bit 15 in the MII control register (0.15) as the reset bit. The bit is self-clearing. Using the aforementioned library, a PHY can be reset with the following code:

	mov	b, #0	;	PHY number
	mov	a, #MII_CONTROL	;	Control register
	call	ETH_ReadMII		
	orl	1, #80h	;	Set reset bit (0.15) in r1
	call	ETH_WriteMII		
reset_wait:				
	call	ETH_ReadMII		
	mov	a, r1		
	jb	acc.7, reset_wait	;	Loop while in reset
reset_wait	orl call : call mov	1, #80h ETH_WriteMII ETH_ReadMII a, rl		

Equivalent code can be written for Java[™] programs running on the TINI[®] Firmware 1.12 and later. com.dalsemi.tininet.TININet contains the readMII and writeMII methods:

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